

1. The first part of the document is a list of references. The references are listed in a standard format, with the author's name, the title of the work, and the publisher. The references are as follows:

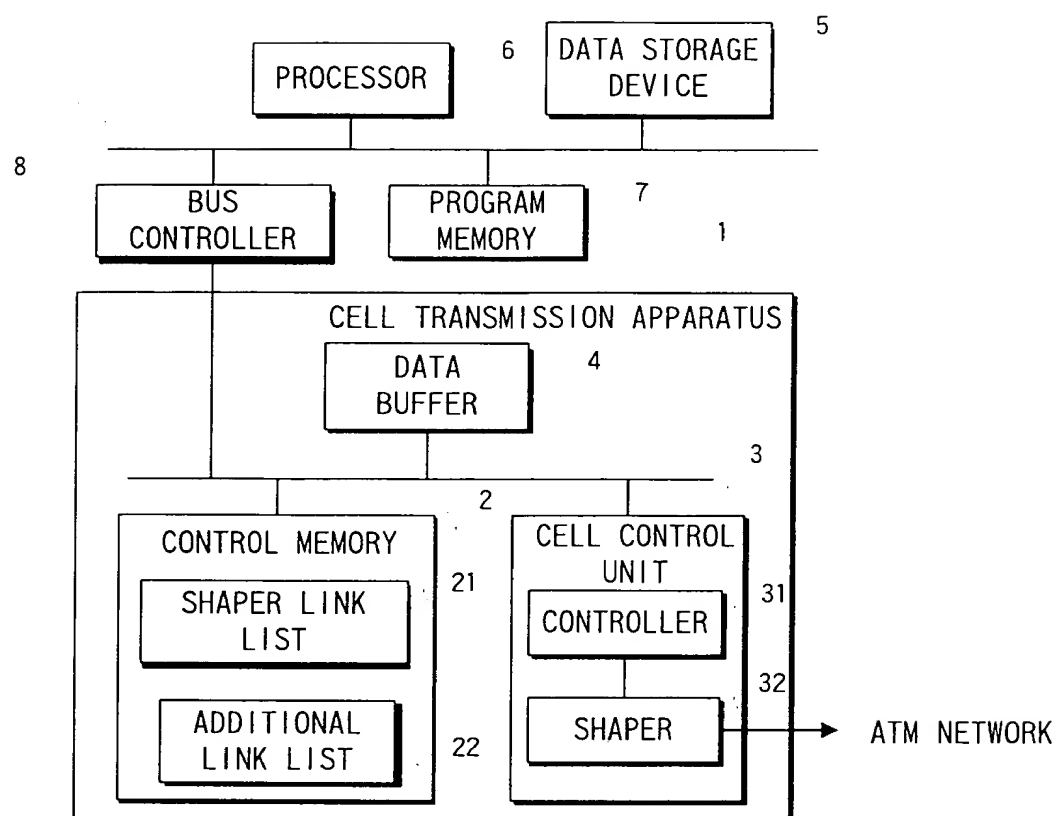


FIG. 1

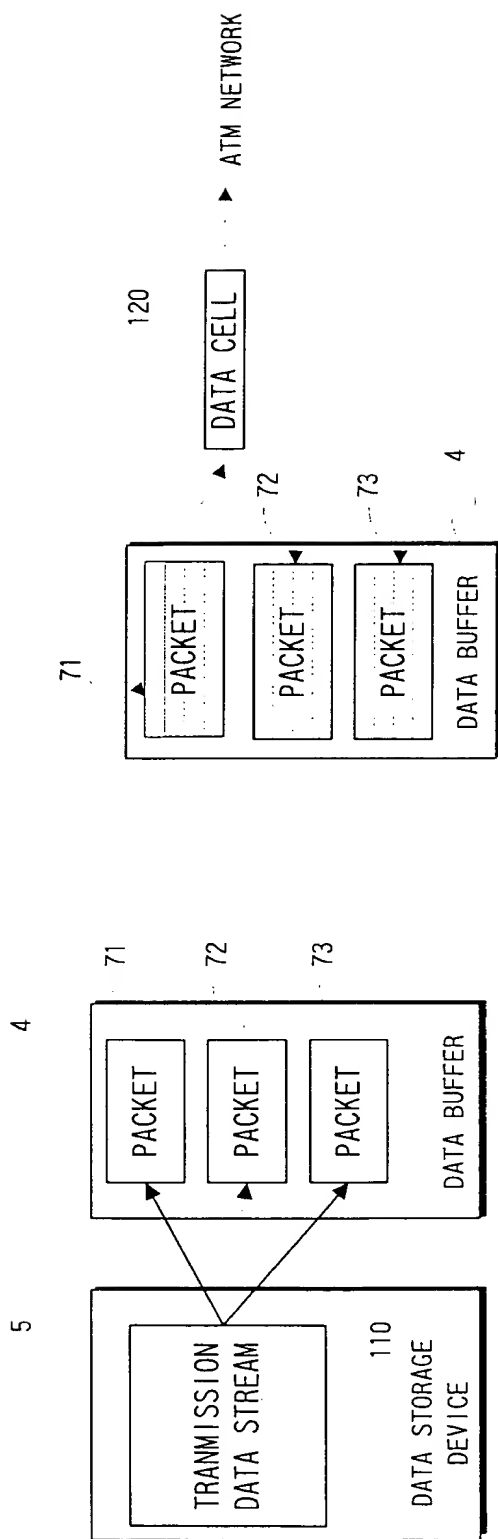
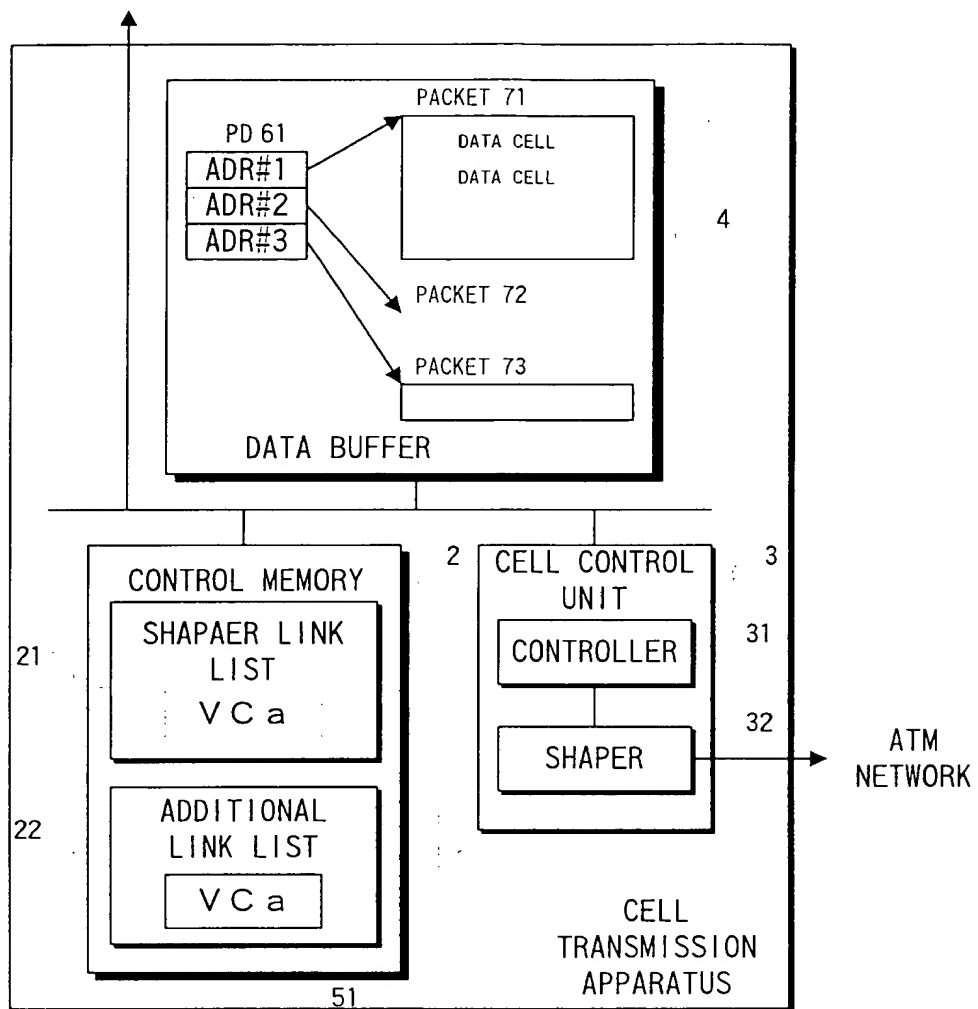


FIG. 2b

FIG. 2a

BUS CONTROLLER 8

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The diagram illustrates the timing of two packets, PACKET 71 and PACKET 72, across a timeline from $t=0$ to $t=32$. The timeline is divided into 8-unit intervals by vertical lines at $t=0, 8, 16, 24, 32$. A horizontal line with arrows at both ends represents the transmission medium. Above this line, 'FIRST SLOT' is indicated with a wavy arrow pointing to the start at $t=0$. 'PACKET 71' is labeled above the line between $t=0$ and $t=24$. 'PACKET 72' is labeled above the line starting at $t=32$. Below the timeline, a bracket from $t=0$ to $t=8$ is labeled 'FIRST TRANSMISSION CYCLE'. Data cells are represented by rectangles: solid black rectangles for 'HEAD DATA CELL' and open rectangles for 'REMAINING DATA CELLS'. For PACKET 71, a head cell is at $t=0$ (labeled 'VCa51' to its left) and three remaining cells are at $t=8, 16, 24$. For PACKET 72, a head cell is at $t=32$. A legend at the bottom right defines the symbols: a solid black rectangle for 'HEAD DATA CELL' and an open rectangle for 'REMAINING DATA CELLS'.

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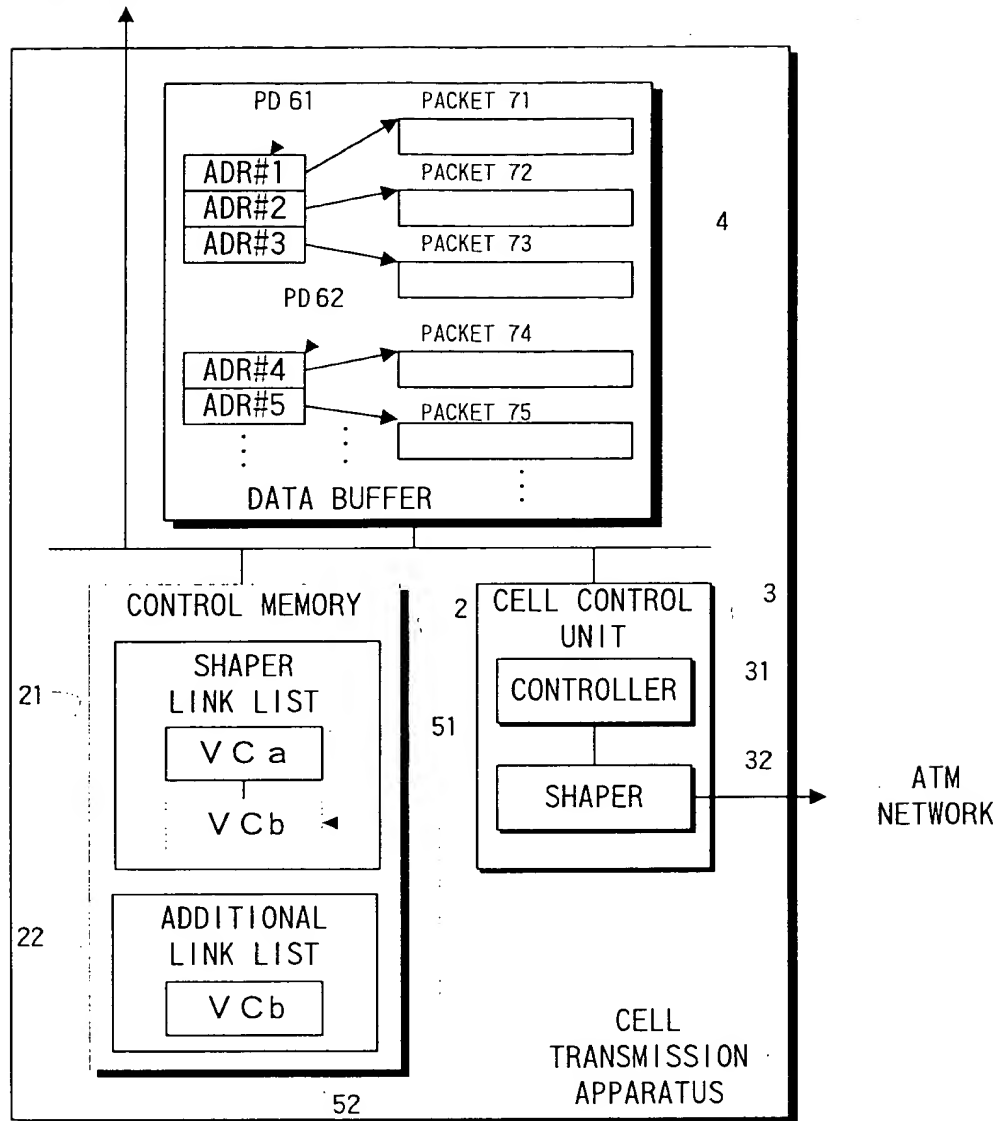


FIG. 6

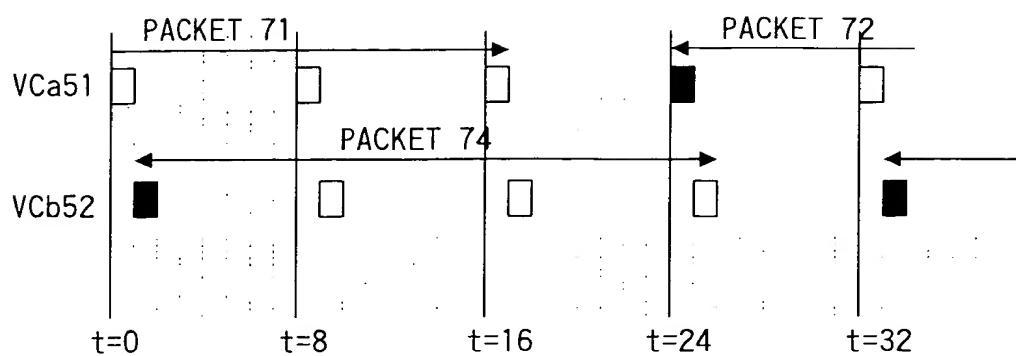


FIG. 7a

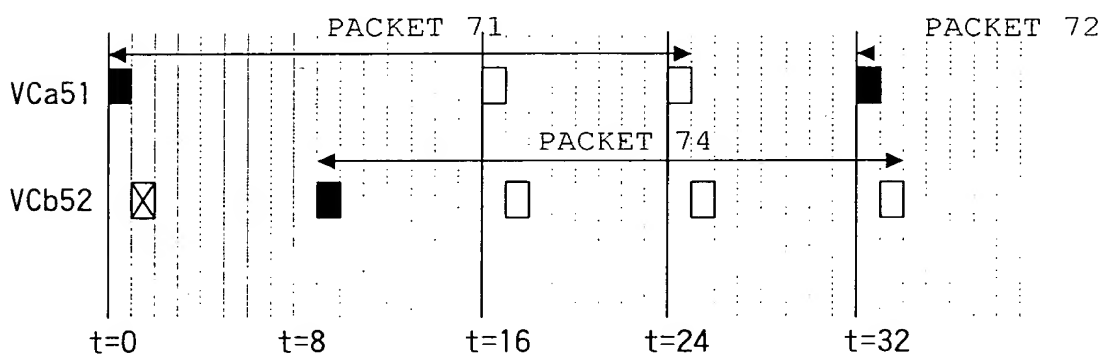


FIG. 7b

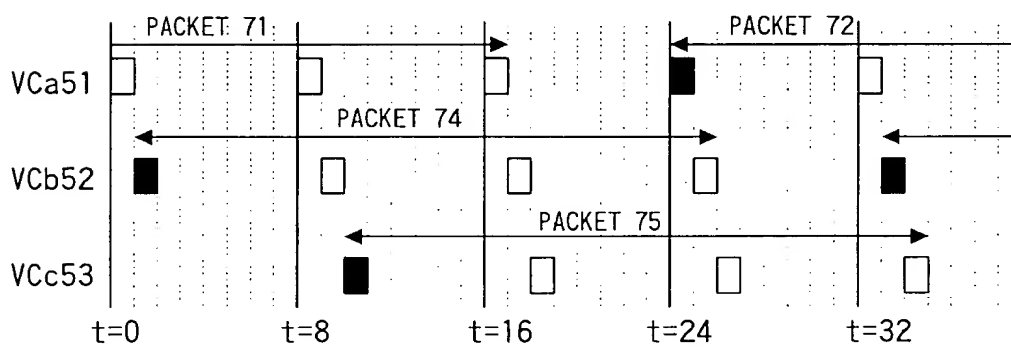
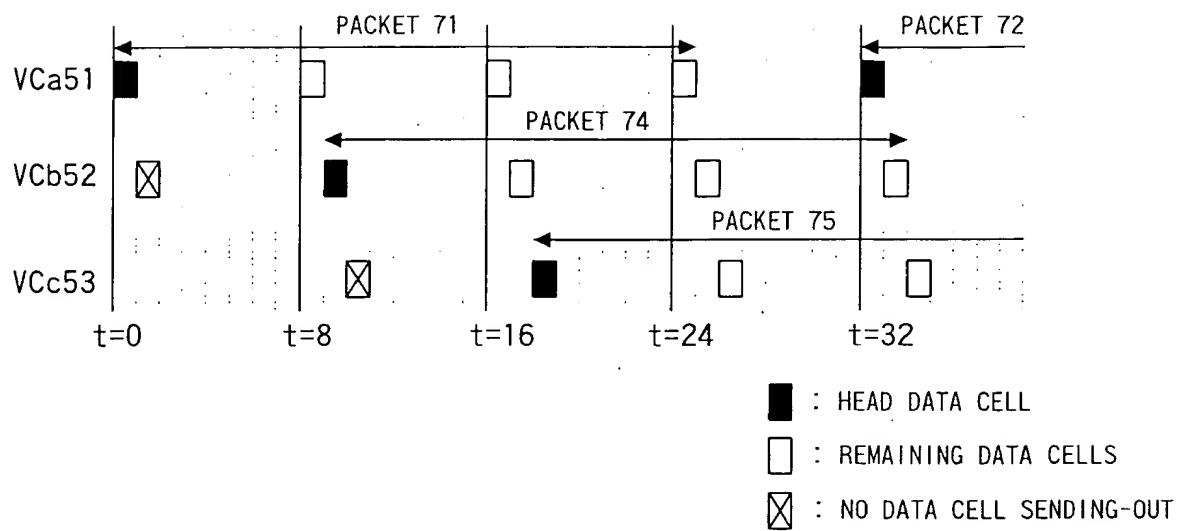
Figure 1 is a block diagram of a cell transmission apparatus. The apparatus is divided into three main sections: a top section for data buffering, a bottom-left section for control memory, and a bottom-right section for cell control.

The top section, labeled "DATA BUFFER", contains three rows of data. Each row has an address field (ADR#1, ADR#4, ADR#6) and a packet field (PACKET 71, PACKET 74, PACKET 75). Arrows point from the address fields to the packet fields.

The bottom-left section, labeled "CONTROL MEMORY", contains two sub-sections: "SHAPER LINK LIST" and "ADDITIONAL LINK LIST". The "SHAPER LINK LIST" contains three entries: "VC a", "VC b", and "VC c". The "ADDITIONAL LINK LIST" contains two entries: "VC b" and "VC c".

The bottom-right section, labeled "CELL CONTROL UNIT", contains a "CONTROLLER" block and a "SHAPER" block. Arrows indicate data flow from the "DATA BUFFER" to the "CELL CONTROL UNIT" and from the "CELL CONTROL UNIT" to the "ATM NETWORK".

FIG. 8



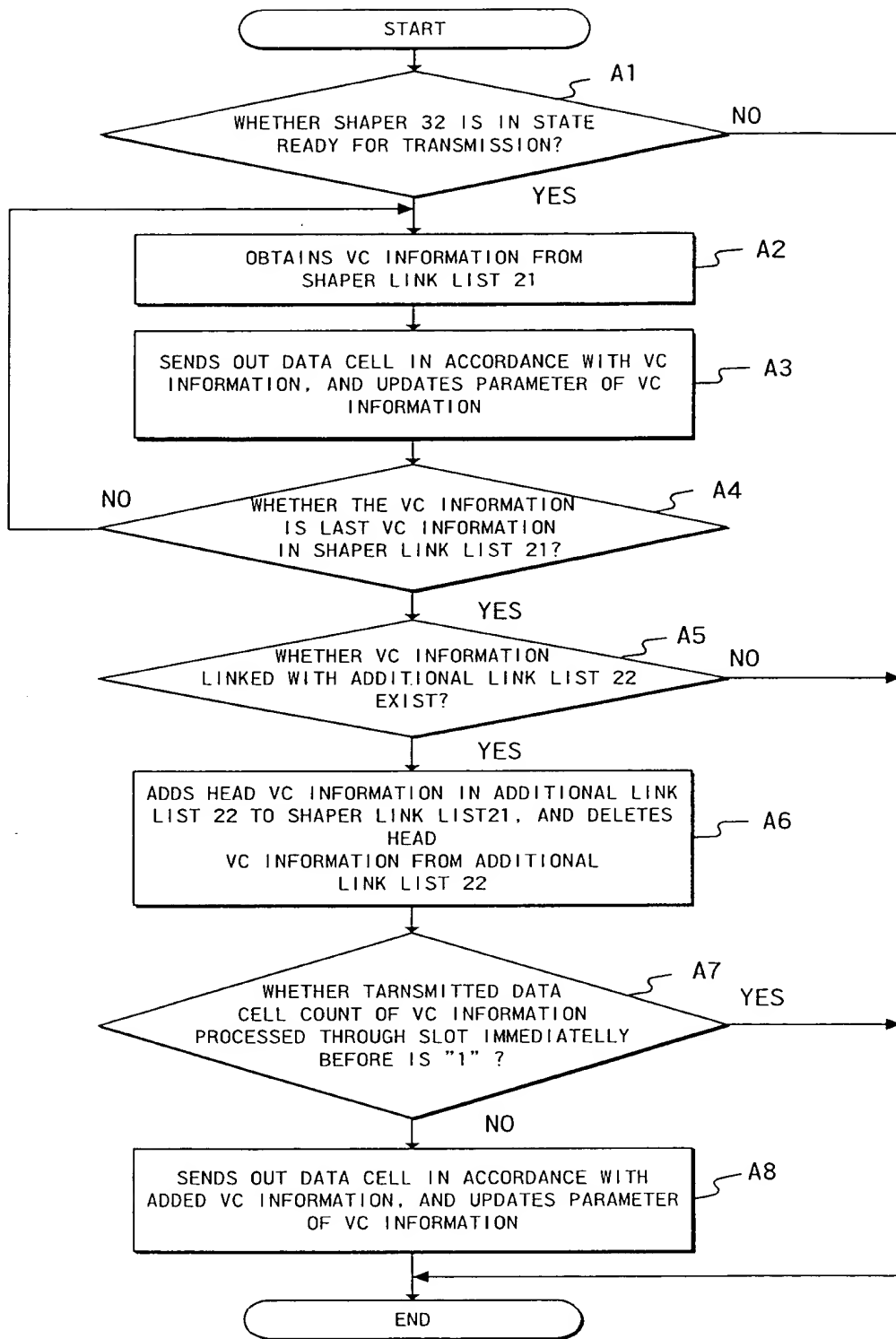


FIG. 10

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graph TD
    Start([START]) --> B1{B1: WHETHER TRANSMITTED DATA CELL COUNT 43 IS "0" ?}
    B1 -- YES --> B2[B2: READ PD ADDRESS 41]
    B1 -- NO --> B4[B4: READS DATA CELL FROM ADDRESS IN DATA BUFFER 4, WHICH IS INDICATED BY READING ADDRESS 42, AND SENDS OUT DATA CELL TO ATM NETWORK]
    B2 --> B3[B3: READS DATA CELL OF PACKET INDICATED BY PD IN DATA BUFFER 4, AND SENDS OUT DATA CELL TO ATM NETWORK]
    B3 --> B5[B5: INCREASES OR RESETS TRANSMITTED DATA CELL COUNT 43, AND UPDATES READING ADDRESS 42 TO NEXT ADDRESS OF SENT DATA CELL]
    B4 --> B5
    B5 --> B6{B6: WHETHER TRANSMITTED DATA CELL COUNT 43 IS "1" ?}
    B6 -- YES --> B7[B7: UPDATES PD ADDRESS 41]
    B6 -- NO --> B4
    B7 --> B5
    B7 --> End([END])

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FIG. 11